SYLLABUS

1. Data about the program of study

1.1 Institution	The Technical University of Cluj-Napoca
1.2 Faculty	Faculty of Automation and Computer Science
1.3 Department	Computer Science
1.4 Field of study	Computer Science and Information Technology
1.5 Cycle of study	Bachelor of Science
1.6 Program of study / Qualification	Computer science / Engineer
1.7 Form of education	Full time
1.8 Subject code	31.

2. Data about the subject

2.1 Subject name	***Structure of Computer Systems***				
2.2 Course responsible / lecturer	Prof. dr. eng. Sebestyen Gheorghe - Gheorghe.Sebestyen@cs.utcluj.ro				
2.3 Teachers in charge of seminars / laboratory / project	Prof. dr. eng. Hângan Anca - anca.hangan@cs.utcluj.ro Lect. dr. eng. Neagu Mădălin - madalin.neagu@cs.utcluj.ro				
2.4 Year of study	III	2.5 Semester	5	2.6 Type of assessment (E - exam, C - colloquium, V - verification)	E
2.7 Subject category	*DF – fundamentală, DD – în domeniu, DS – de specialitate, DC – complementară*				DD
	DI – Impusă, DOp – opțională, DFac – facultativă				DI

3. Estimated total time

3.1 Number of hours per week	5	of which:	Course	2	Seminars	-	Laboratory	2	Project	1
3.2 Number of hours per semester	70	of which:	Course	28	Seminars	-	Laboratory	28	Project	14
3.3 Individual study:										
(a) Manual, lecture material and notes, bibliography										20
(b) Supplementary study in the library, online and in the field										17
(c) Preparation for seminars/laboratory works, homework, reports, portfolios, essays										15
(d) Tutoring										0
(e) Exams and tests										3
(f) Other activities:										0

3.4 Total hours of individual study (suma (3.3(a)...3.3(f)))	55
3.5 Total hours per semester (3.2+3.4)	125
3.6 Number of credit points	5

4. Pre-requisites (where appropriate)

4.1 Curriculum	Digital system design, Computer architecture
4.2 Competence	Understand and operate with basic concepts regarding computer system's hardware

5. Requirements (where appropriate)

5.1. For the course	
5.2. For the applications	

6. Specific competence

6.1 Professional competences	**C2** – Designing hardware, software and communication components (5 credits) • **C2.1** – Describing the structure and functioning of computational, communication and software components and systems • **C2.2** – Explaining the role, interaction and functioning of hardware, software and communication components • **C2.3** – Building the hardware and software components of some computing systems using algorithms, design methods, protocols, languages, data structures, and technologies • **C2.4** – Evaluating the functional and non-functional characteristics of the computing systems using specific metrics • **C2.5** – Implementing hardware, software and communication systems
6.2 Cross competences	N/A

7. Discipline objective (as results from the *key competences gained*)

7.1 General objective	The main goal of the course is to present in an accessible way advanced design methods and techniques used in today's microprocessors and computer systems
7.2 Specific objectives	To study: Methods and metrics for computer performance assessment Advanced CPU designs (pipelining, multicore, parallele and distributed computing) Memory hierarchies: cache memory, virtual memory, new DRAM technologies RISC architecture Parallel computers architectures – hardware issues and solutions

8. Contents

8.1 Lectures	Hours	Teaching methods	Notes
Introduction. Computer Performance Parameters and Methods of Improvement	2	Lecture based on slides, onsite	
Computer performance and optimality, Benchmarking	2		
The Arithmetical and Logical Unit (ALU)	2		
The Central Processing Unit (CPU) – MIPS architecture, pipeline, hazard cases	2		
The Central Processing Unit – advance techniques: Scoreboard method, Tomasulo's algorithm, Branch prediction techniques	2		
The Central Processing Unit – multi-core systems	2		
Microprocessors – basic components and advanced implementations	2		
Memory System – memory technologies (SRAM, DRAM) and design principles	2		
Memory Hierarchies – cache and virtual memory	2		
Interconnection Systems – serial and parallel synchronous and asynchronous buses, multipoint interconnections	2		
Parallel Computer Architectures - different levels of parallel execution	2		
RISC Architectures – principles and implementation examples	2		
Distributed Computing – GRID and Cloud Systems	2		
Technological Perspectives in Computer Architectures	2		

Bibliography:

1. Gorgan Dorian, Sebestyen Gheorghe, Structura Calculatoarelor, Editura albastra, Cluj-Napoca 2005
2. Hennessy John, Patterson David, Computer architecture, a Quantitative Approach, Ed. Elsevier, 2007
3. Baruch, Z. F., Structure of Computer Systems, U.T.PRES, Cluj-Napoca, 2002, ISBN 973-8335-44-2.

8.2 Applications - Seminars / Laboratory / Project	Hours	Teaching methods	Notes
Measuring the performance of computer systems with benchmarks	2		

Measuring the performance of computer systems with benchmarks	2		
CPU performance measurement using the Time-Stamp Counter register	2		
Programming elements in VHDL	2		
Design of ALU components	2		
FPGA Synthesis	2		
Streaming Data Processing. AXI4-Stream Communication Protocol	2		
Streaming Data Processing. Design of AXI4-Stream Compliant Modules	2		
Streaming Data Processing. Use-Case: Anomaly Detection in Sensor Data	2		
Procedures of data processing compliant with AXI4-Stream on an FPGA development board.	2		
SRAM and DRAM memory design - 2	2		
Design of high-speed memories	2		
Directly mapped cache memory implementation	2		
Review exercises	2		
Laboratory examination	2		

Bibliography:

1. Laboratory works available on Moodle
2. Intel, Using the RDTSC Instruction for Performance Monitoring [accessed Sept. 2024], https://www.ccsl.carleton.ca/~jamuir/rdtscpm1.pdf
3. Peter Kankowski, Performance measurements with RDTSC [accessed Sept. 2024], https://www.strchr.com/performance_measurements_with_rdtsc
4. John Lyon-Smith, Getting accurate per thread timing on Windows [accessed Sept. 2024], https: //web.archive.org/web/20090510073435/http://lyon-smith.org/blogs/code-o-rama/archive/2007/07/17/timing-code-on-windows-with-the-rdtsc-instruction.aspx
5. AMBA 4 AXI4-Stream Protocol Specification - Arm [accessed Oct. 2024], https://documentation-service.arm.com/static/642583d7314e245d086bc8c9?token=
6. How the axi-style ready/valid handshake works [accessed Oct. 2024], https://vhdlwhiz.com/how-the-axi-style-ready-valid-handshake-works/
7. Vivado Design Suite User Guide: Designing with IP (UG896) - Using the IP Catalog [accessed Oct. 2024], https://docs.xilinx.com/r/en-US/ug896-vivado-ip/Using-the-IP-Catalog
8. Stimulus file read in testbench using TEXTIO [accessed Oct. 2024], https://vhdlwhiz.com/stimulus-file/
9. Crockett, L. H., Elliot, R. A., Enderwitz, M. A., & Stewart, R. W. (n.d.). *The Zynq book: Embedded processing with the ARM® Cortex®-A9 on the Xilinx® Zynq®-7000 all programmable SoC* (1st ed.). Department of Electronic and Electrical Engineering, University of Strathclyde
10. Z.F. Baruch, *Aplicatii de Proiectare Digitala cu Circuite FPGA*, ISBN 978-606-020-261-5,2020
11. AMD, „7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide (UG480)", Sept. 2022. *[Online]. Available*: https://docs.amd.com/r/en-US/ug480_7Series_XADC/XADC-Overview

**Se vor preciza, după caz: tematica seminariilor, lucrările de laborator, tematica și etapele proiectului.*

9. Bridging course contents with the expectations of the representatives of the community, professional associations and employers

The content of the course has been aligned with similar courses from the USA and Europe, as well as with the content of well-established textbooks used in prestigious universities. Additionally, the course content has been discussed with representatives of companies from Romania and the USA. The course has been evaluated by the ARACIS agency.

10. Evaluation

Activity type	Assessment criteria	Assessment methods	Weight in the final grade
Course	Theoretical knowledge level	Written exam, onsite	60%

Seminar	-	-	-
Laboratory	Hardware Design skills	Practical evaluation, onsite	20 %
Project			20 %
Minimum standard of performance: Minimum 5 for the Course and for the Application assessment Grade calculus: 60% written exam + 20% laboratory evaluation + 20% project evaluation Conditions for participating in the final exam: Laboratory ≥ 5, Project ≥ 5 Conditions for promotion: final grade ≥ 5			

Date of filling in: 26.02.2025	**Responsible**	**Title, First name Last name**	**Signature**
	Course	Prof.dr.eng. Gheorghe SEBESTYEN	
	Applications	Prof.dr.eng. Anca HÂNGAN	
		Lect.dr.eng. Mădălin NEAGU	

Date of approval in the department	Head of department, Prof.dr.eng. Rodica Potolea
Date of approval in the Faculty Council	Dean, Prof.dr.eng. Vlad Mureșan