SYLLABUS

1. Data about the program of study

1.1 Institution	The Technical University of Cluj-Napoca
1.2 Faculty	Faculty of Automation and Computer Science
1.3 Department	Computer Science
1.4 Field of study	Computer Science and Information Technology
1.5 Cycle of study	Bachelor of Science
1.6 Program of study / Qualification	Computer science / Engineer
1.7 Form of education	Full time
1.8 Subject code	23.

2. Data about the subject

2.1 Subject name			Computer Architecture				
2.2 Course responsible / lecturer			Prof.di	Prof.dr.eng. Oniga Florin - Florin.Oniga@cs.utcluj.ro			
			Assoc.	Assoc.prof.dr.eng. Negru Mihai - Mihai.Negru@cs.utcluj.ro			
			Lect.dr.eng. Vancea Cristian-Cosmin - <u>Cristian.Vancea@cs.utcluj.ro</u>				
2.3 Teachers in charge of	.3 Teachers in charge of seminars / Prof.dr.eng. Oniga Florin - Florin.Oniga@cs.utcluj.ro						
laboratory / project			Assoc.	prof.	dr.eng. Negru Mihai - Mihai.Negru@cs.utcluj.ro		
			Lect.dr	eng.	Vancea Cristian-Cosmin - <u>Cristian.Vancea@cs.utcluj.ro</u>		
			Assoc.prof.dr.eng. Itu Răzvan - Razvan.Itu@cs.utcluj.ro				
			Lect.dr.eng. Lişman Florin Dragoş - <u>Dragos.Lisman@cs.utcluj.ro</u>				
			Lect.dr.eng. Nandra Constantin - Constantin.Nandra@cs.utcluj.ro				
			Lect.dr.eng. Mureşan Mircea-Paul - Mircea.Muresan@cs.utcluj.ro				
			As.eng	. Atti	la Ernő Füzes - <u>Attila.Fuzes@cs.utcluj.ro</u>		
			As.eng	. Vivi	an Chiciudean - <u>Vivian.Chiciudean@cs.utcluj.ro</u>		
2.4 Year of study	II	II 2.5 Semester 2 2 2.6 Type of assessment (E - exam, C - colloquium, V - verification)		E			
2.7 Subject category		fundame	entală, L	DD — 1	n domeniu, DS – de specialitate, DC – complementară	DD	
		mpusă, l	pusă, DOp – opțională, DFac – facultative			DI	

3. Estimated total time

3.1 Number of hours per week	4	of which:	Course	2	Seminars	-	Laboratory	2	Project	-
3.2 Number of hours per semester	56	of which:	Course	28	Seminars	1	Laboratory	28	Project	-
3.3 Individual study:										
(a) Manual, lecture material an	d note	s, bibliogra	phy							28
(b) Supplementary study in the library, online and in the field						14				
(c) Preparation for seminars/laboratory works, homework, reports, portfolios, essays						23				
(d) Tutoring							0			
(e) Exams and tests							4			
(f) Other activities:						0				
3.4 Total hours of individual study (su	ıma (3.	3(a)3.3(f))))		69					
3.5 Total hours per semester (3.2+3.4) 125										

4. Pre-requisites (where appropriate)

3.6 Number of credit points

4.1 Curriculum	Logic design >= 5, Digital system design >= 5
4.2 Competence Ability to design digital circuits and to implement them in VHDL	

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1/4

5. Requirements (where appropriate)

5.1. For the course	blackboard, video projector, laptop
5.2. For the applications	desktop/laptop computer, Xilinx Vivado, FPGA development boards

6. Specific competence

6.1 Professional competences	 C2 – Designing hardware, software and communication components C2.1 - Describing the structure and functioning of computational, communication and software components and systems C2.2 - Explaining the role, interaction and functioning of hardware, software and communication components C2.3 - Building the hardware and software components of some computing systems using algorithms, design methods, protocols, languages, data structures, and technologies C2.4 - Evaluating the functional and non-functional characteristics of the computing systems using specific metrics C2.5 - Implementing hardware, software and communication systems
6.2 Cross competences	N/A

7. Discipline objective (as results from the key competences gained)

7.1 General objective	Knowing and understanding the concepts of organization and functioning fo central processing units, memories, input/output, and using these concepts fo design.		
7.2 Specific objectives	 Applying methods for representation and design at system level for digital circuits Instruction Set Architecture specification Writing simple programs in assembly languages and machine code Specification, design, implementation, and testing of central processing units, micro-architectures, data paths, command units Understanding memory organization Understanding modern trends in computer architectures 		

8. Contents

8.1 Lectures	Hours	Teaching methods	Notes
Introduction	2		
High-Level Synthesis	2	1	
Instruction Set Architecture	2	1	
CPU Design – Single Cycle CPU	2	1	
Computer Arithmetic and Simple Arithmetic Logic Units	2	Oral presentation	
CPU Design – Multi Cycle CPU Data path	2	multimedia equipment, interactive communication, blackboard problem	
CPU Design – Multi Cycle CPU Control	2		
CPU Design – Pipelined CPU. Hazards	2		
Dynamic Scheduling of the Execution	2		
Speculative execution and Branch Prediction	2	solving	
Memory	2	1	
Modern CPU Architectures	2]	
Problem solving	2	1	
Problem solving	2	1	
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Bibliography:

- 1. D. A. Patterson, J. L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 5th edition, Morgan–Kaufmann, 2013, and newer editions.
- 2. J. L. Hennessy, D. A. Patterson, "Computer Organization and Design: A Quantitative Approach", 5th edition, Morgan–Kaufmann, 2011, and newer editions.

- 3. F. Oniga, "De la bit la procesor. Introducere în arhitectura calculatoarelor", U.T. Press, 2019, ISBN 978-606-737-366-0, disponibil online, Romanian only.
- 4. W. Stallings, "Computer Organization and Architecture", 11th edition, global edition, Pearson, 2021.
- 5. S. L. Harris, D. M. Harris, "Digital Design and Computer Architecture", RISC-V edition, Morgan-Kaufmann, 2021.
- 6. MIPS Technologies, Inc., "MIPS32 Architecture for Programmers, Volume I: Introduction to the MIPS 32™ Architecture".
- 7. MIPS Technologies, Inc., "MIPS32 Architecture for Programmers, Volume II: The MIPS 32™ Instruction Set".

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8.2 Applications - Seminars / Laboratory / Project	Hours	Teaching methods	Notes
Introduction in the Vivado environment	2		
Design and Implementation of arithmetic-logic unit	2		
Design and Implementation of memory components	2		
Design of a Single Cycle MIPS – Introduction	2		
Design of a Single Cycle MIPS – Instruction fetch	2	Blackboard quick	
Design of a Single Cycle MIPS – Instruction decode and control	overview of key issues,	exercises,	
Design of a Single Cycle MIPS – Architecture completion	2	experimenting with	
Midterm practical evaluation on the FPGA board	2	FPGA development	
Pipelined MIPS CPU Design – Implementation	2	boards with specialized	
Pipelined MIPS CPU Design – Hazard detection and correction	2	IDEs for circuit design and implementation	
Pipelined MIPS CPU Design	2		
Serial peripheral interfacing	2	1	
Practical evaluation of the pipelined MIPS CPU on the FPGA board	2]	
Final Tests and Evaluation	2]	
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Bibliography: Online bibliography

- 1. M. Negru, F. Oniga, C. Vancea, Laboratory Guide https://mihai.utcluj.ro/computer-architecture, https://users.utcluj.ro/~vcristian/AC.html
- 2. F. Oniga, M. Negru, "Arhitectura Calculatoarelor Îndrumător de laborator", U.T. Press, 2019, ISBN 978-606-737-350-9.
- 3. M. Negru, F. Oniga, S. Nedevschi, "Computer Architecture Laboratory Guide", U.T. Press, 2019, ISBN 978-606-737-123-9.

9. Bridging course contents with the expectations of the representatives of the community, professional associations and employers in the field

Computer Architecture is one of the fundamental subjects of the Computer Science and Information Technology field. It combines fundamental and practical aspects used for digital circuits design and implementation. The content of this subject is harmonized with the specific curricula of other national and international universities and is evaluated by the Romanian government agencies (CNEAA and ARACIS). The practical aspects involve getting familiar with and using development products and tools provided by companies from Romania, Europe, and USA (ex. Xilinx, Digilent).

10. Evaluation

Activity type	Assessment criteria	Assessment methods	Weight in the final grade
Course	Testing the theoretical knowledge, the ability of problem solving, presence and activity	Written exam	50%
Laboratory	Practical ability to solve and implement specific problems related to processor design, presence and activity	Lab exam, periodical assessment of results	50%
Project	-	-	-

Minimum standard of performance:

Knowing the fundamental theory of the subject, the ability to design and implement a processor with a reduced set of instructions.

Conditions for participating in the final exam: Lab ≥ 5

Conditions for promotion: Final exam ≥ 5 Grade calculus: 50% lab + 50% final exam

Date of filling in: Responsible 26.02.2025		Title, First name Last name	Signature
26.02.2025	Course	Prof.dr.eng. Florin ONIGA	
		Assoc.prof.dr.eng. Mihai NEGRU	
		Lect.dr.eng. Cristian-Cosmin VANCEA	
	Applications	Prof.dr.eng. Florin ONIGA	
		Assoc.prof.dr.eng. Mihai NEGRU	
		Lect.dr.eng. Cristian-Cosmin VANCEA	
		Assoc.prof.dr.eng. Răzvan ITU	
		Lect.dr.eng. Florin-Dragoş LIŞMAN	
		Lect.dr.eng. Constantin NANDRA	
		Lect.dr.eng. Mircea-Paul MUREŞAN	
		As.eng. Attila Ernő FÜZES	
		As.eng. Vivian CHICIUDEAN	

Date of approval in the department	Head of department, Prof.dr.eng. Rodica Potolea
Date of approval in the Faculty Council	Dean, Prof.dr.eng. Vlad Mureșan